

PATENT ABSTRACTS OF JAPAN

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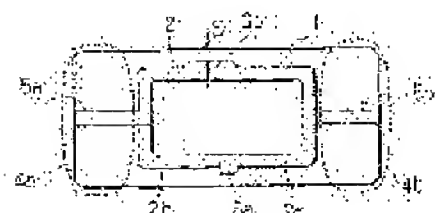
25. 12. 2003

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(54) LAMINATED CHIP INDUCTOR



(57)Abstract:

PROBLEM TO BE SOLVED: To provide a laminated chip inductor that can improve Q characteristics.

SOLUTION: An insulating layer comprising a magnetic material or a non-magnetic material wherein conductor patterns 2a and 2b are formed or the non-magnetic material is stacked while the conductor patterns 2a and 2b for the respective layers are connected by a through hole, and a continuous coil conductor 2 is formed in the laminate. Leading conductors 5a and 5b on both ends of the coil conductor 2 are connected with terminal electrodes 4a and 4b on both ends being at a right angle in the lamination direction of the laminate 1. The width of a pattern in junctions 6a and 7a with the through hole in the conductor patterns 2a and 2b of the respective layers connected by the through hole is made wider than those of the conductor patterns 2a and 2b, and the pattern is

formed as projecting outward from the outer edge of the conductor patterns 2a and 2b. Thus, a flux generating in the coil conductor 2 is prevented from blocking the passage at the junctions 6a and 7a, resulting in the improved Q characteristics.

LEGAL STATUS

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application]

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CLAIMS

[Claim(s)]

[Claim 1]

while connecting by the through hole and carrying out the laminating of between the conductor patterns which formed in each class the insulating layer which consists of the magnetic substance or non-magnetic material in which the conductor pattern was formed -- a coiled form continuous

inside a layered product -- a conductor -- forming -- this coiled form --
- the drawer of the ends of a conductor -- the laminating mold chip
inductor which comes to connect a conductor with the terminal electrode
of the both ends which make the direction of a right angle in the
direction of a laminating of said layered product -- it is
The laminating mold chip inductor characterized by the width of face of
the pattern of a joint with said through hole in the conductor pattern
of each class connected by said through hole being larger than the width
of face of said conductor pattern, and projecting outside the rim of a
conductor pattern, and forming it.

[Claim 2]

In a laminating mold chip inductor according to claim 1,
said coiled form -- the configuration where the conductor was seen
through in the direction of a laminating -- a rectangle or an ellipse --
nothing and this coiled form -- the laminating mold chip inductor
characterized by forming the joint with said through hole in the long
side of a conductor.

[Claim 3]

In a laminating mold chip inductor according to claim 1,
said coiled form -- the configuration where the conductor was seen
through in the direction of a laminating -- a rectangle or an ellipse --
nothing and this coiled form -- a part or all of a joint with said
through hole forms in the short side part or the arc section of a
conductor -- having

It is the laminating mold chip inductor characterized by for said
terminal electrode not covering said conductor pattern when it saw
through and sees in the direction of a laminating, but having wrap
structure for a part of lobe [at least] to the outside of a joint with
said through hole.

[Claim 4]

In a laminating mold chip inductor according to claim 1 to 3,
The laminating mold chip inductor characterized by forming the area of a
joint with said through hole in a twice [more than] as many size as
the cross-sectional area of a through hole.

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DETAILED DESCRIPTION

[Detailed Description of the Invention]

[Field of the Invention]

[0001]

the conductor pattern formed in each class in the insulating layer which this invention becomes from the magnetic substance or non-magnetic material in which the conductor pattern was formed -- a through hole -- minding -- connecting -- a laminating -- carrying out -- the interior of a layered product -- a coiled form -- the laminating mold chip inductor in which the conductor was formed is started, and it is related with the structure which raised especially the Q factor.

[Background of the Invention]

[0002]

the conventional laminating mold chip inductor is shown in drawing 10 or drawing 11 -- as -- the inside of a layered product 11 -- a coiled form -- the width of face W1 of the joint 16 with the through hole 13 established in the edge of the conductor patterns 12a and 12b which form a conductor 12 forms more widely than the width of face W2 (refer to drawing 12 (A)) of conductor patterns 12a and 12b. and the joint 16 of such a through hole 3 -- a coiled form -- it is made to project inside a conductor 12 and is prepared. In addition, in drawing 10 and drawing 11, 14 is the terminal electrode prepared in the ends of a layered product 1. There is patent reference 1 as an example which adopted the structure of such a joint 16. Moreover, as another example, as shown in drawing 12 (B), the structure where the joint 16 of a through hole 13 was made to project in the inside-and-outside both directions of a layered product 11 may be adopted. As shown in drawing 12 (C), there is also an example which made the joint 16 with a through hole 13 equal to the width of face of conductor patterns 12a and 12b (patent reference 2 reference).

[0003]

Thus, the reason for forming the joint 16 with a through hole 13 broadly By establishing a through hole 13 in a ceramic green sheet, and printing after that the conductive paste which becomes with the paste containing silver dust etc. While forming conductor patterns 12a and 12b, in case

it is filled up with conductive paste in a through hole 13 It is for preventing the location gap with a through hole 13 and a joint 16 as compared with the case where a joint 16 is formed in conductor patterns 12a and 12b and equal width, as shown in drawing 12 (C), and this preventing an open circuit.

[0004]

[Patent reference 1] JP, 2002-15918, A

[Patent reference 2] JP, 2001-126726, A

[Description of the Invention]

[Problem(s) to be Solved by the Invention]

[0005]

when a joint 16 is formed more broadly than conductor patterns 12a and 12b and it is made to project inside a layered product 11 as shown in drawing 12 (A) and (B), it is shown in drawing 13 -- as -- the joint 16 with a through hole 13 -- a coiled form -- transparency of the flux F generated in a conductor 12 is checked, and there is a trouble of reducing Q which is the essential property of a coil.

[0006]

This invention aims at offering the laminating mold chip inductor of a configuration of that it becomes possible to raise a Q factor in view of the above-mentioned trouble.

[Means for Solving the Problem]

[0007]

(1) while it connects by the through hole and the laminating mold chip inductor of this invention carries out the laminating of between the conductor patterns which formed in each class the insulating layer which consists of the magnetic substance or non-magnetic material in which the conductor pattern was formed -- a coiled form continuous inside a layered product -- a conductor -- forming -- this coiled form -- the drawer of the ends of a conductor -- the laminating mold chip inductor which comes to connect a conductor with the terminal electrode of the both ends which make the direction of a right angle in the direction of a laminating of said layered product -- it is

The width of face of the pattern of a joint with said through hole in the conductor pattern of each class connected by said through hole is larger than the width of face of said conductor pattern, and is characterized by being projected and formed outside the rim of a conductor pattern.

[0008]

(2) Set the laminating mold chip inductor of this invention above (1), said coiled form -- the configuration where the conductor was seen

through in the direction of a laminating -- a rectangle or an ellipse -- nothing and this coiled form -- it is characterized by forming the joint with said through hole in the long side of a conductor.

[0009]

(3) Moreover, set the laminating mold chip inductor of this invention above (1),

said coiled form -- the configuration where the conductor was seen through in the direction of a laminating -- a rectangle or an ellipse -- nothing and this coiled form -- a part or all of a joint with said through hole forms in the short side part or the arc section of a conductor -- having

When it saw through and sees in the direction of a laminating, said terminal electrode does not cover said conductor pattern, but it is characterized by having wrap structure for a part of lobe [at least] to the outside of a joint with said through hole.

[0010]

(4) Moreover, set the laminating mold chip inductor of this invention to the above (1) thru/or either of (3),

It is characterized by forming the area of a joint with said through hole in a twice [more than] as many size as the cross section of a through hole.

[Effect of the Invention]

[0011]

since the laminating mold chip inductor of this invention was formed broadly, without making it project outside the rim of a conductor pattern, and making a joint with the through hole of a conductor pattern project inside -- a coiled form -- the degree which checks the flux generated with a conductor by the joint with a through hole decreases substantially. For this reason, it becomes possible to raise Q which is the essential property of a coil.

[0012]

moreover, said coiled form -- the configuration where the conductor was seen through in the direction of a laminating -- a rectangle or an ellipse -- carrying out -- this coiled form -- when a joint with said through hole is formed in the long side of a conductor, a conductor pattern is exposed to the side face (cutting plane) of a layered product, or the degree which a terminal electrode connects with a conductor pattern too hastily decreases substantially, and the yield improves.

[0013]

moreover, said coiled form -- when a conductor makes a rectangle or an ellipse, it sees through in the direction of a laminating, and said

conductor pattern cannot be covered, but the degree of capacity coupling between the joints of wrap structure then a terminal electrode, and a through hole can decrease in a part of lobe [at least] to the outside of a joint with said through hole, and said terminal electrode can control lowering of self-resonant frequency (SRF).

[0014]

Moreover, by making area of a joint with a through hole into twice [more than (preferably 4 or less times)] the cross section of a through hole, each other gap generated from the location precision of a through hole and location precision, such as screen-stencil, can be absorbed, and the open circuit as a coil can be prevented.

[Best Mode of Carrying Out the Invention]

[0015]

Drawing 1 is drawing which saw through and looked at the gestalt of 1 operation of the laminating mold chip inductor by this invention in the direction of a laminating. the coiled form by which 1 was formed in the layered product and 2 was formed into it in drawing 1 -- it is a conductor and is shown in laminating structural drawing of drawing 2 -- as -- said coiled form -- a conductor 2 is constituted by connecting the conductor patterns 2a-2f of 1 / 2 turn structures by through holes 3a-3e. 4a and 4b are the terminal electrodes prepared in the both ends of the longitudinal direction which makes an abbreviation right angle in the direction of a laminating of a layered product 1, and the conductor patterns 2a and 2f of the ends of the direction of a laminating pull them out to these terminal electrodes 4a and 4b, and they are connected to Conductors 5a and 5b, respectively.

[0016]

6a-6e are joints formed simultaneously with conductor patterns 2a-2e on said through hole 3a - 3e. 7a-7e are joints which said through holes 3a-3e pile up by the laminating. As it represents with conductor pattern 2b in drawing 3 and is shown in it, these joints 6a-6e, and 7a-7e set up widely Joints 6a-6e and the width of face W4 of 7a-7e from width-of-face W3 of conductor patterns 2a-2e, so that a part may not project outside a conductor patterns [2a-2f] rim at the projection inside. desirable -- said joints 6a-6e and the area (L-W4) of 7a-7e -- the cross section of through holes 3a-3e -- Joints 6a-6e and the location gap with 7a-7e are preferably prevented as 4 or less times more than twice.

[0017]

This laminating mold chip inductor opens through holes 3a-3e in the green sheet which prepares two or more ceramic green sheets 1a-1j for picking, among those forms the insulating layers 1c-1g for conductor

pattern 2a-2f. Next, conductor patterns 2a-2f are printed with the conductive paste which becomes a green sheet equivalent to insulating layers 1c-1h from silver or a ****-strike. In the case of the printing, the laminating of the conductive paste is filled up with and carried out to through holes 3a-3e. Then, it calcinates in the temperature and the environment of having been suitable for the metal-powder ingredient which used, having cut in all directions, and it can be burned, conductive paste is made ends, and it electroplates after that for soldering.

[0018]

thus -- if the joints 6a-6e with through holes 3a-3e, and 7a-7e are made into the broad configuration which projected on the outside of a layered product 1 -- a coiled form -- since the degree by which passage of the flux generated in a conductor 2 is barred by Joints 6a-6e, and 7a-7e decreases substantially, Q value improves.

[0019]

[when it designs so that spacing S may be formed between Joints 6a (-6e) and 7a (-7e) and the side faces of a layered product 1 which were established in the long side of a conductor 2] moreover, the coiled form which makes a rectangle temporarily as shown in drawing 1 -- structure is followed conventionally and it is shown in drawing 4 -- as -- spacing S and the same spacing -- a coiled form, when it constitutes so that it may be formed between the side faces of a conductor 2 and a layered product 1 As a conductor pattern shows a two-dot chain line by the blot of a conductor pattern and the gap of a pattern by printing, it exposes to the side face of a layered product 1, or possibility of connecting with the terminal electrodes 4a and 4b too hastily becomes large.

[0020]

the coiled form which will make a rectangle on the other hand if the structure of the gestalt of this operation is adopted -- since the broad joints 6a-6e, and 7a-7e are formed in a part of long side of a conductor, a conductor is exposed to the side face of a layered product 1, or possibility of connecting with the terminal electrodes 4a and 4b too hastily becomes very small, and the yield improves substantially. said joints 6a-6e, and 7a-7e -- a coiled form -- although you may prepare in the edge of the long side of a conductor 2 -- these joints 6a-6e, and 7a-7e -- a coiled form -- it is desirable to prepare near the center of the long side of a conductor 2 in the semantics which lessens possibility of a conductor patterns [by said blot etc. / the terminal electrodes 4a and 4b and conductor patterns 2a-2f] short circuit.

[0021]

moreover, the coiled form which sees in the direction of a laminating and makes a rectangle so that drawing 1 may show -- the shorter side side of a conductor 2 is not covered with the terminal electrodes 4a and 4b -- as -- a coiled form -- arranging a conductor 2 -- a coiled form -- the degree of capacity coupling of a conductor 2 and the terminal electrodes 4a and 4b can decrease, and lowering of SRF can be prevented.

[0022]

Drawing 5 is the gestalt of other operations of this invention, and drawing 6 is the layer structural drawing. the insulating layer from which 1a-1i constitute a layered product 1 in drawing 5 and drawing 6 , and 2g-2k -- a coiled form -- the conductor pattern which constitutes a conductor 2 every 1/2 turn -- 4c pulls out 3f-3i, and conductor patterns 2g and 2k pull out a through hole and 4d. Conductor 5c, A joint with the through hole formed of printing with the terminal electrode which connects 5d, and the conductive paste with which the part of through holes 3f-3i is filled up with 6f-6i, and 7f-7i are joints to which through holes 3f-3i are joined by the laminating.

[0023]

the coiled form which looks at these joints 6f-6i, and 7f-7i in the direction of a laminating unlike the gestalt of said operation, and makes a rectangle -- the short side part of a conductor 2 -- a coiled form -- it is formed so that a part may project outside the rim of a conductor 2. Moreover, as shown in drawing 5 , it sees through in the direction of a laminating, and said terminal electrodes 4c and 4d do not cover the short side part of said conductor patterns 2g-2k, but have wrap structure for a part of joint 6f-6i with said through holes 3f-3i, and lobe [at least] to the outside of 7f-7i. The laminating mold chip inductor of the gestalt of this operation is also produced by said same manufacture approach.

[0024]

thus -- if constituted -- the gestalt of said operation -- the same -- Joints 6f-6i, and 7f-7i -- a coiled form -- since it does not project inside a conductor 2, the degree of flux, Joints 6f-6i, and the passage inhibition by 7f-7i decreases, and improvement in Q can be attained. Moreover, the degree of the joints 6f-6i of the terminal electrodes 4c and 4d and a through hole and capacity coupling between 7f-7i can decrease, and lowering of SRF can be prevented.

[0025]

Drawing 7 is the gestalt of other operations of this invention, and drawing 8 is the layer structural drawing. the insulating layer from

which 1a-1j constitute a layered product 1 in drawing 7 and drawing 8 , and 2m-2r -- a coiled form -- the conductor pattern which constitutes a conductor 2 every 3/4 turn -- 4e pulls out 3j-3n, and conductor patterns 2m and 2r pull out a through hole and 4f. Conductor 5e, A joint with the through hole formed with the terminal electrode which connects 5f, and the conductive paste with which a through holes [3j-3n] part is filled up 6j-6n, 7j-7n are joints to which through holes 3j-3n are joined by the laminating. the coiled form which sees in the direction of a laminating these joints 6j-6n and 7j-7n unlike the gestalt of said operation, and makes a rectangle -- the both sides of the short side part and long side of a conductor 2 -- a coiled form -- it is formed so that a part may project outside the rim of a conductor 2.

[0026]

Moreover, as shown in drawing 7 , it sees through in the direction of a laminating, and said terminal electrodes 4e and 4f do not cover said conductor patterns 2m-2r, but have wrap structure for a part of said through holes [3j-3n] joint 6j-6n and lobe [at least] to an outside (7j-7n). The laminating mold chip inductor of the gestalt of this operation is also produced by said same manufacture approach.

[0027]

Also in the gestalt of this operation, improvement in Q and the depressor effect of lowering of SRF as well as the gestalt of said operation are obtained. moreover -- according to the gestalt of operation of drawing 7 and drawing 8 -- the gestalt of operation of drawing 1 and drawing 2 -- comparing -- a coiled form -- joint 6j from the long side of a conductor 2 -- The number of turns of the number of projection (7j, 6l., 7l., 6n, and 7n) (in the case of 3.5 turns and drawing 8 , it is 4.5 when it is ****2****) decreases comparatively (in the case of drawing 2 , they are six pieces when the numbers of projection of the joint in a long side are ten pieces and drawing 8), and improvement in the yield can be expected.

[0028]

moreover -- even if it compares with the gestalt of operation of drawing 5 and drawing 6 -- a coiled form -- the joints [in the short side part of a conductor 2 / 6k, 7k, 6m, and 7m] number of projection also decreases considering the number of turns (in the case [In the case of drawing 6] of drawing 8 2.5 turn, 4.5 turn), and becomes high as compared with the case where the depressor effect of SRF lowering is drawing 5 and drawing 6 .

[0029]

the coiled form at the time of seeing through in the direction of a

laminating in the gestalt of said the operation of each -- although the configuration of a conductor 2 was made into the rectangle, it is good also as an ellipse.

[0030]

the structure of this invention -- the conventional laminating mold chip inductor -- comparing -- a coiled form -- the thing of the former [locate / a conductor 2 / inside the periphery side of a layered product 1] -- a coiled form -- a conductor -- since the line length of the 2 whole becomes a little short, speaking of an inductance value, it is suitable when applying to what acquires a comparatively small inductance value (an inductance value is 10 or less nHs).

[Example]

[0031]

(Example 1) Many alumina 30wt% things containing the ceramic constituent of a presentation were used as a ceramic green sheet for picking glass 70wt% which consists of strontium, calcium, an alumina, and oxidation silicon. After forming the through holes 3a-3e for [this] realizing the configuration of the gestalt of operation of drawing 1 and drawing 2 to the green sheet for picking, while printing conductor patterns 2a-2f to the green sheet for many picking which corresponds, respectively, it was filled up with much silver pastes by printing of a silver paste in said through holes 3a-3e. After carrying out the laminating of these green sheets, it cut to the chip simple substance so that a completion dimension might be set to 1005 (1.0mm, width of face, and height are 0.5mm for a long side), and calcinated at 900 degrees C. Then, the silver paste used as the substrate layer of the terminal electrodes 4a and 4b was burned at 700 degrees C, and nickel and Sn were further put with electroplating. Conductor patterns [after baking / 2a-2f] width of face 50 micrometers, Joints 6a-6e, 80 micrometers and conductor patterns [2a-2f] thickness for the width of face of 7a-7e 12 micrometers, a coiled form -- 320 micrometers and the direction of a short hand the bore of a conductor 2 150 micrometers [a longitudinal direction] Thickness of the part between which the conductor patterns [in / for the thickness of the insulating layers 1a-1j between which conductor patterns 2a-2f are not made to be placed / 30 micrometers and insulating layers 1c-1j] 2a-2f were made to be placed was set to 20 micrometers, and the number of turns was set to 3.5, and it constituted so that an inductance value might serve as 3.3nH(s).

[0032]

Moreover, as an example of a comparison, Joints 6a-6e and width of face of 7a-7e should be made to be the same as that of the above, the

projection direction should be carried out inside, and other configurations were made the same as said example, and constituted the inductor.

[0033]

Drawing 9 is a graph which shows the result of having measured Q value in the range of 10 to 3000MHz about said Example A and example B of a comparison. When being based on the example of this invention so that clearly from drawing 9, as compared with the example of a comparison, Q value is excellent from 6 ten in the frequency range (800-3000MHz) used with a cellular phone.

[0034]

(Example 2)

the inductor which takes the structure of the gestalt of operation shown in drawing 5 and drawing 6 -- setting -- a coiled form -- that from which the width of face of a conductor 2 and the number of turns are made the same as said example 1, and an inductance value serves as 3.3nH(s) -- setting -- a coiled form -- the location of a conductor 2 -- changing

(1) When it sees through in the direction of a laminating and Joints 6f-6i, and 7f-7i are not covered with the terminal electrodes 4c and 4d

(2) When it sees through in the direction of a laminating and a part of Joints 6f-6i and 7f-7i are covered with the terminal electrodes 4c and 4d

(3) When it sees through in the direction of a laminating and Joints 6f-6i and all of 7f-7i are covered with the terminal electrodes 4c and 4d
When it was alike, it attached and SRF was investigated, respectively, in the case of (1), in the case of :6.8GHz and (2), the result of :5.9GHz was obtained in the case of :6.3GHz and (3), and the important thing became clear in the semantics in which lessening the degree with which a joint is covered with the terminal electrodes 4c and 4d prevents lowering of SRF.

[Brief Description of the Drawings]

[0035]

[Drawing 1] It is drawing which saw through and looked at the gestalt of 1 operation of the laminating mold chip inductor by this invention in the direction of a laminating.

[Drawing 2] It is layer structural drawing of the laminating mold chip inductor of drawing 1 .

[Drawing 3] It is the top view showing the structure of a joint with the through hole of the laminating mold chip inductor of drawing 1 .

[Drawing 4] It is the explanatory view of the conductor pattern of the

example of a comparison.

[Drawing 5] It is drawing which saw through and looked at the gestalt of other operations of the laminating mold chip inductor by this invention in the direction of a laminating.

[Drawing 6] It is layer structural drawing of the laminating mold chip inductor of drawing 5 .

[Drawing 7] It is drawing which saw through and looked at the gestalt of other operations of the laminating mold chip inductor by this invention in the direction of a laminating.

[Drawing 8] It is layer structural drawing of the laminating mold chip inductor of drawing 7 .

[Drawing 9] It is the graph which compares and shows the Q value to the frequency of the example of this invention, and the example of a comparison.

[Drawing 10] It is drawing which saw through and looked at an example of the conventional laminating mold chip inductor in the direction of a laminating.

[Drawing 11] It is drawing which saw through and looked at other examples of the conventional laminating mold chip inductor in the direction of a laminating.

[Drawing 12] (A), (B), and (C) are drawings showing a joint with the through hole of the conventional laminating mold chip inductor.

[Drawing 13] It is drawing showing the flow of the flux in the conventional laminating mold chip inductor.

[Description of Notations]

[0036]

1: a layered product, a 1a-1j:insulating layer, and 2:coiled form -- a conductor, a 2a-2r:conductor pattern, a 3a-3n:through hole, a 4a-4f:terminal electrode, and a 5a-5f:drawer -- a conductor, 6a-6n, and a 7a-7n:joint

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DESCRIPTION OF DRAWINGS

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[Drawing 13] It is drawing showing the flow of the flux in the conventional laminating mold chip inductor.

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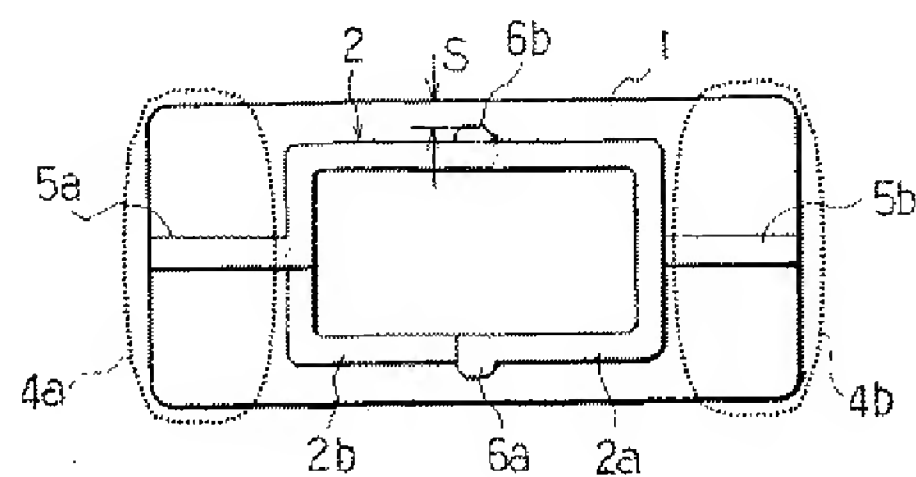
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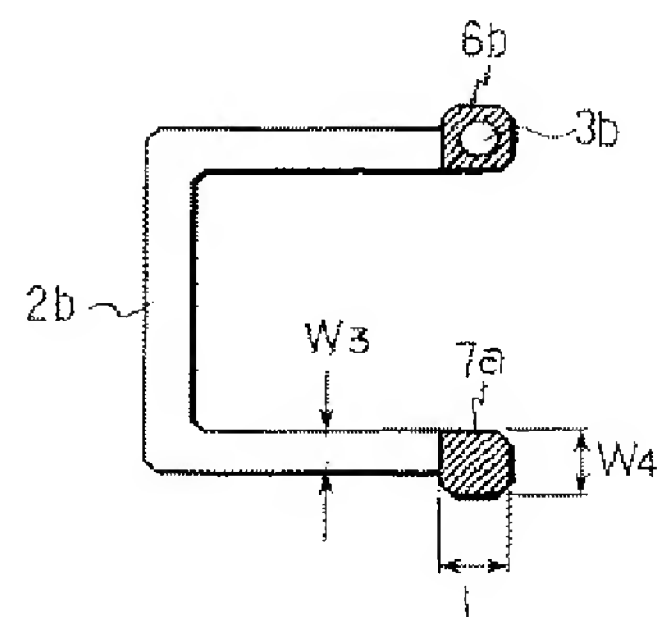
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DRAWINGS

[Drawing 1]

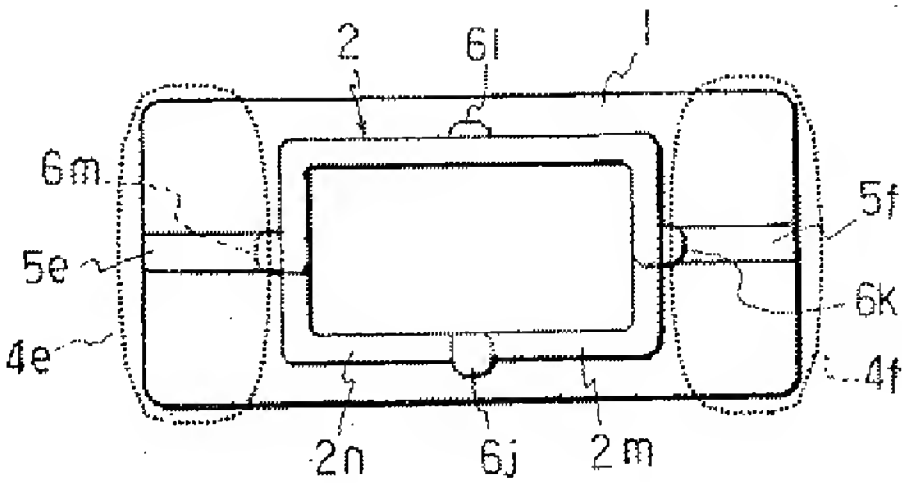


[Drawing 3]

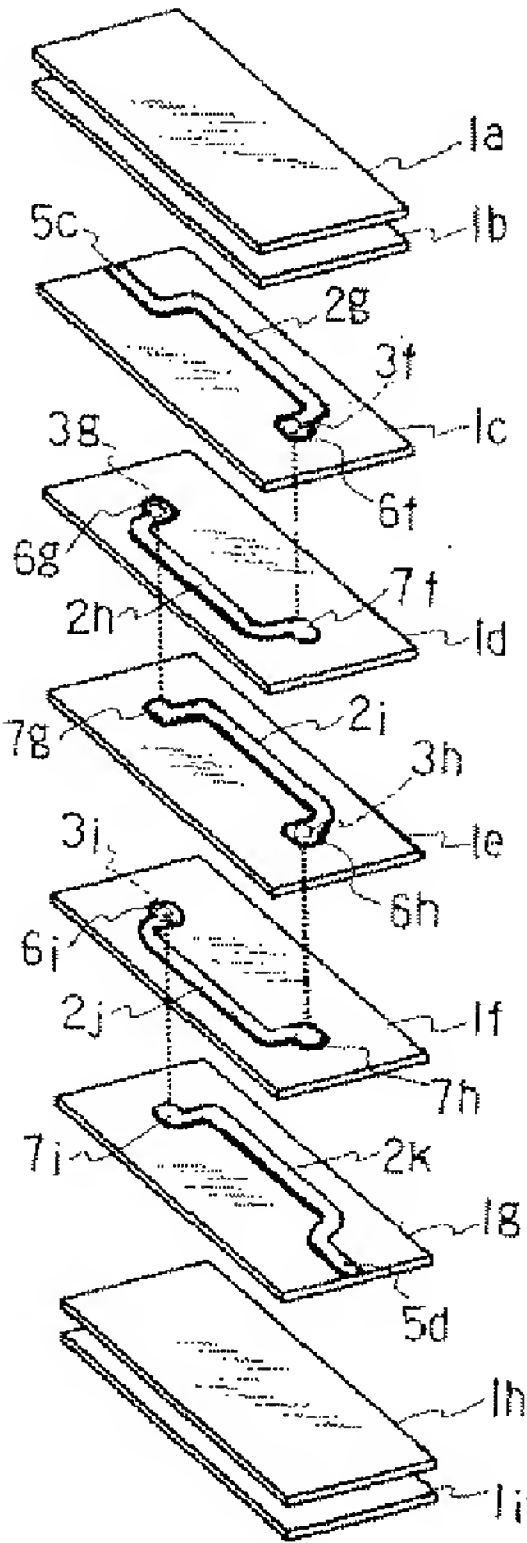


[Drawing 2]

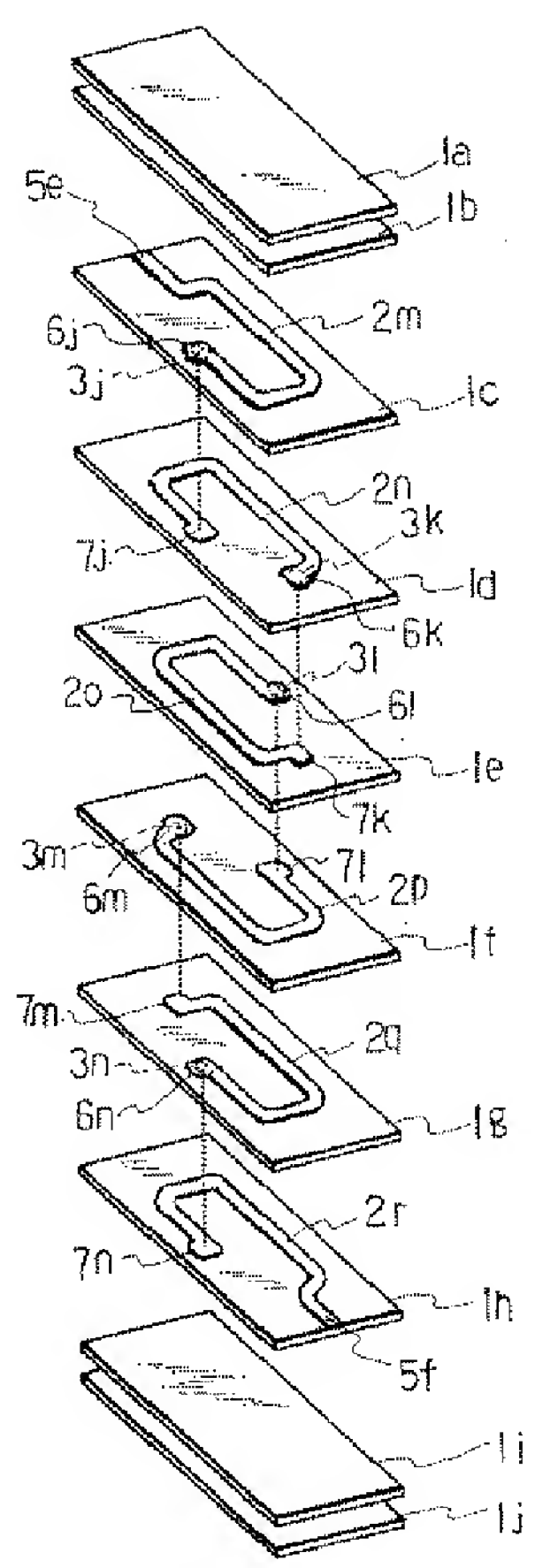
[Drawing 7]



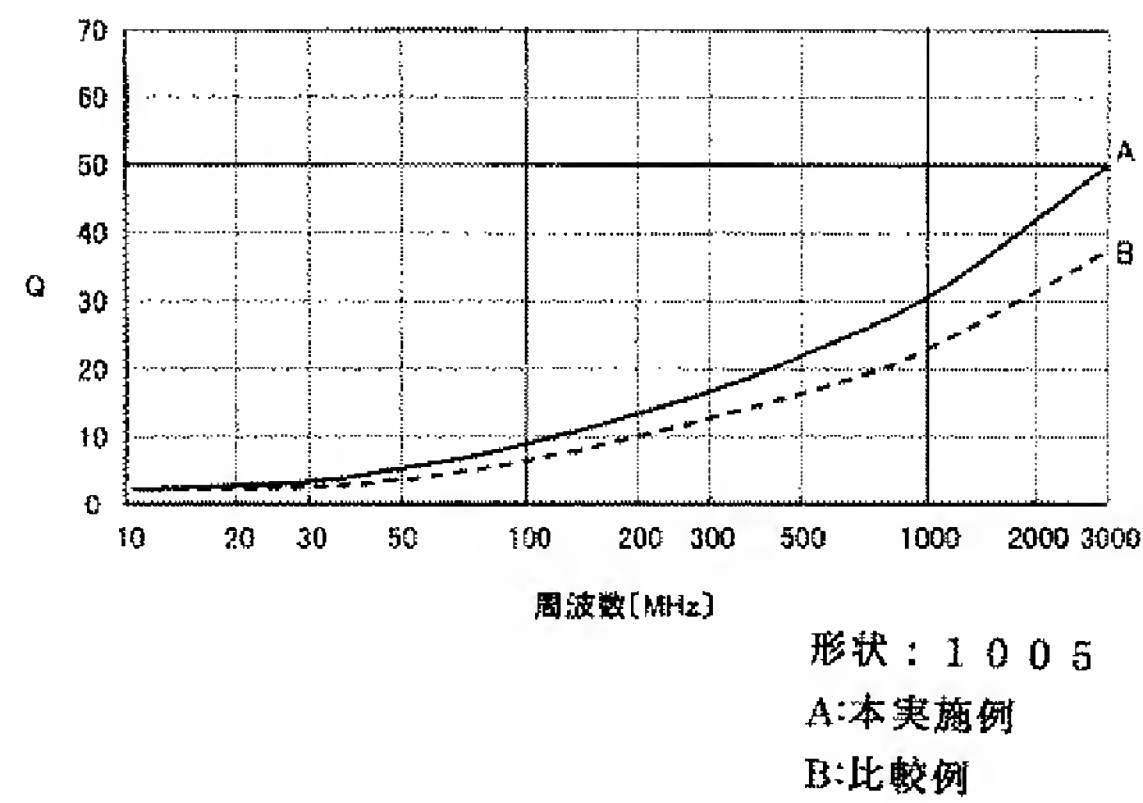
[Drawing 6]



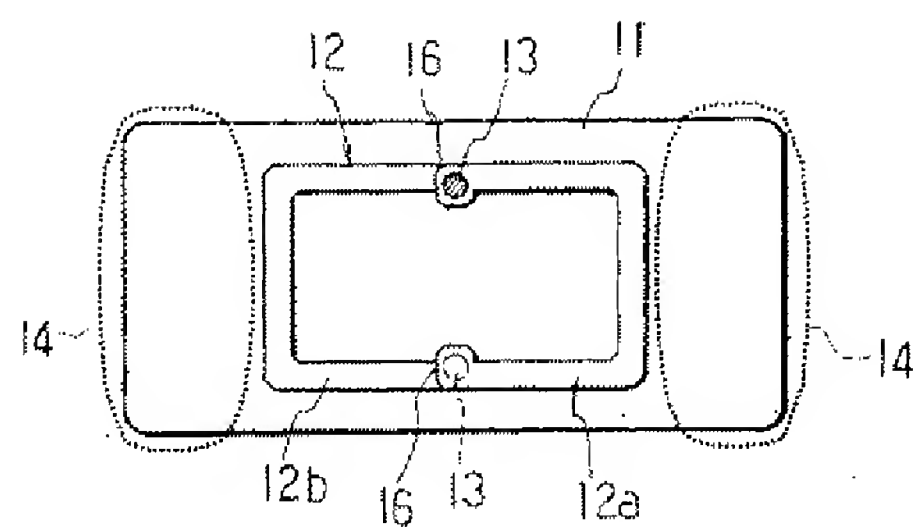
[Drawing 8]



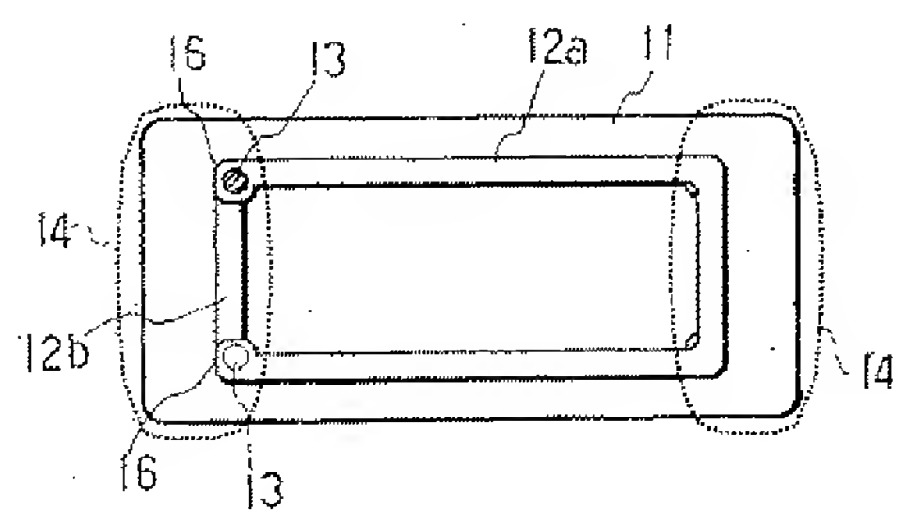
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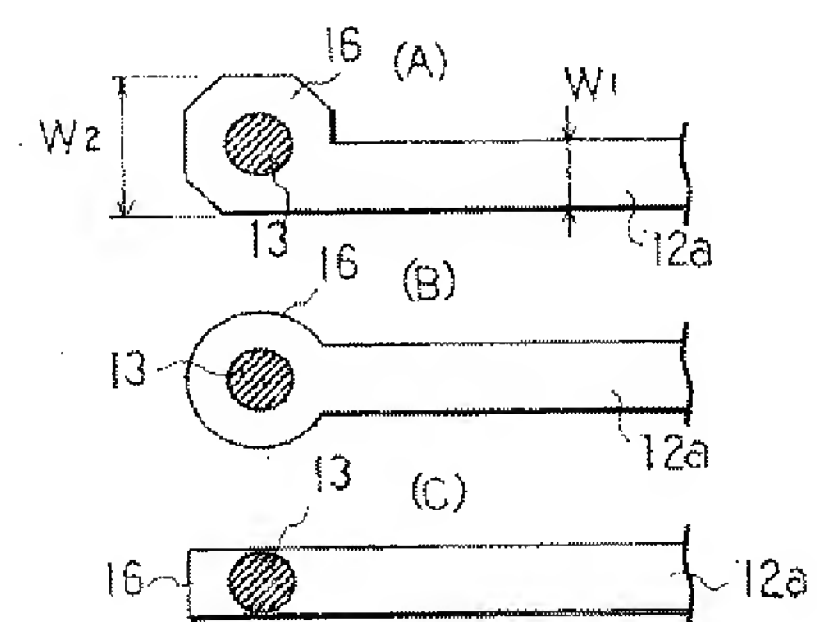
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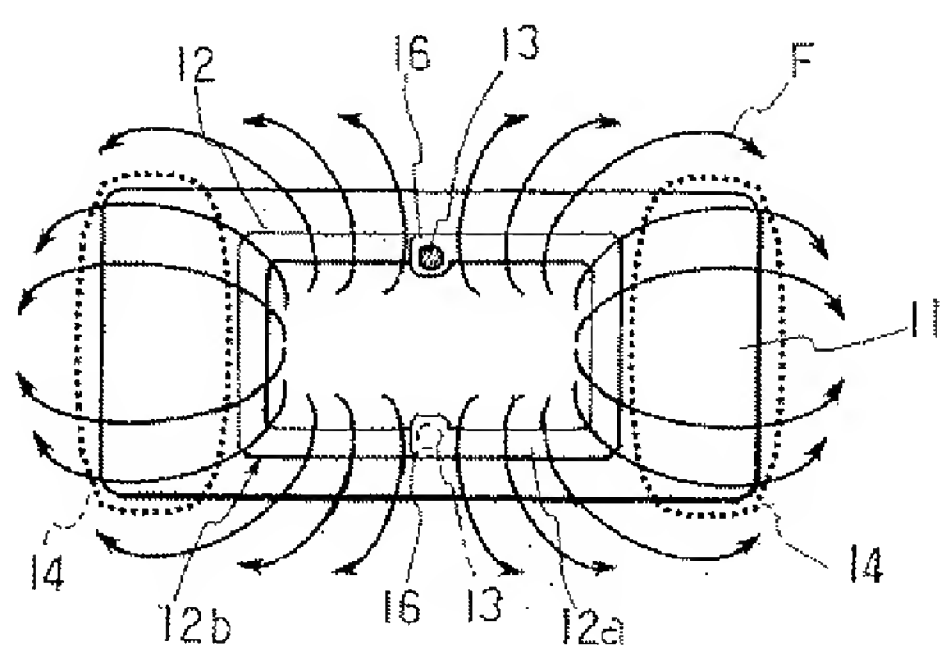
[Drawing 11]



[Drawing 12]



[Drawing 13]



[Translation done.]

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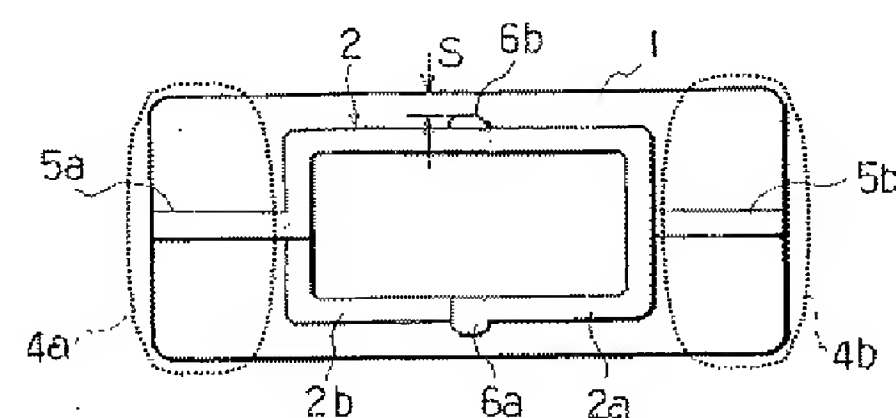
(54) 【発明の名称】 積層型チップインダクタ

(57) 【要約】

【課題】 Q特性を向上させることが可能となる構成の積層型チップインダクタを提供する。

【解決手段】 導体パターン2a、2bを形成した磁性体または非磁性体からなる絶縁層を、各層の導体パターン2a、2b間をスルーホールにより接続して積層すると共に、該積層体内部に連続的なコイル状導体2を形成する。コイル状導体2の両端の引き出し導体5a、5bを、積層体1の積層方向に直角方向をなす両端部の端子電極4a、4bに接続する。スルーホールにより接続される各層の導体パターン2a、2bにおけるスルーホールとの接合部6a、7aのパターンの幅を、導体パターン2a、2bの幅より大きく、かつ導体パターン2a、2bの外縁より外側に突出して形成する。これによりコイル状導体2で発生するフラックスが接合部6a、7aの通過を阻害する度合いが減少しQが向上する。

【選択図】 図1



【特許請求の範囲】

【請求項1】

導体パターンを形成した磁性体または非磁性体からなる絶縁層を、各層に形成した導体パターン間をスルーホールにより接続して積層すると共に、積層体内部に連続的なコイル状導体を形成し、該コイル状導体の両端の引き出し導体を、前記積層体の積層方向に直角方向をなす両端部の端子電極に接続してなる積層型チップインダクタであって、

前記スルーホールにより接続される各層の導体パターンにおける前記スルーホールとの接合部のパターンの幅が、前記導体パターンの幅より大きく、かつ導体パターンの外縁より外側に突出して形成されていることを特徴とする積層型チップインダクタ。

【請求項2】

請求項1に記載の積層型チップインダクタにおいて、

前記コイル状導体を積層方向に透視した形状が長方形または長円形をなし、該コイル状導体の長辺部に前記スルーホールとの接合部が形成されていることを特徴とする積層型チップインダクタ。

【請求項3】

請求項1に記載の積層型チップインダクタにおいて、

前記コイル状導体を積層方向に透視した形状が長方形または長円形をなし、該コイル状導体の短辺部または弧状部に前記スルーホールとの接合部の一部または全部が形成され、

積層方向に透視して見た場合、前記端子電極は前記導体パターンを覆わず、前記スルーホールとの接合部の外側への突出部の少なくとも一部を覆う構造を有することを特徴とする積層型チップインダクタ。

【請求項4】

請求項1ないし3のいずれかに記載の積層型チップインダクタにおいて、

前記スルーホールとの接合部の面積がスルーホールの断面積の2倍以上の広さに形成されていることを特徴とする積層型チップインダクタ。

【発明の詳細な説明】

【技術分野】

【0001】

本発明は、導体パターンを形成した磁性体または非磁性体からなる絶縁層を、各層に形成された導体パターンがスルーホールを介して接続して積層し、積層体の内部にコイル状導体を形成した積層型チップインダクタに係り、特にそのQ特性を向上させた構造に関する。

【背景技術】

【0002】

従来の積層型チップインダクタは、図10または図11に示すように、積層体11内にコイル状導体12を形成する導体パターン12a、12bの端部に設けられるスルーホール13との接合部16の幅W1が、導体パターン12a、12bの幅W2（図12（A）参照）より広く形成している。そして、このようなスルーホール13の接合部16はコイル状導体12の内側に突出させて設けられる。なお、図10、図11において、14は積層体1の両端に設けた端子電極である。このような接合部16の構造を採用した例として、例えば特許文献1がある。また、別の例として、図12（B）に示すように、スルーホール13の接合部16を積層体11の内外両方向に突出させた構造を採用される場合もある。図12（C）に示すように、スルーホール13との接合部16を導体パターン12a、12bの幅に等しくした例もある（特許文献2参照）。

【0003】

このように、スルーホール13との接合部16を幅広に形成する理由は、セラミックグリーンシートにスルーホール13を設け、その後、銀粉を含むペースト等なる導体ペーストを印刷することにより、導体パターン12a、12bを形成すると共にスルーホール13内に導体ペーストを充填する際に、図12（C）に示すように接合部16を導体パターン12a、12bと等幅に形成する場合に比較し、スルーホール13と接合部16との

位置ずれを防止し、これにより、断線を防止するためである。

【0004】

【特許文献1】特開2002-15918号公報

【特許文献2】特開2001-126726号公報

【発明の開示】

【発明が解決しようとする課題】

【0005】

図12(A)、(B)に示したように、接合部16を導体パターン12a、12bより幅広に形成して積層体11の内側に突出させた場合、図13に示すように、スルーホール13との接合部16がコイル状導体12において発生するフラックスFの透過を阻害し、コイルの重要特性であるQを低下させてしまうという問題点がある。

【0006】

本発明は、上記問題点に鑑み、Q特性を向上させることが可能となる構成の積層型チップインダクタを提供することを目的とする。

【課題を解決するための手段】

【0007】

(1) 本発明の積層型チップインダクタは、導体パターンを形成した磁性体または非磁性体からなる絶縁層を、各層に形成した導体パターン間をスルーホールにより接続して積層すると共に、積層体内部に連続的なコイル状導体を形成し、該コイル状導体の両端の引き出し導体を、前記積層体の積層方向に直角方向をなす両端部の端子電極に接続してなる積層型チップインダクタであって、

前記スルーホールにより接続される各層の導体パターンにおける前記スルーホールとの接合部のパターンの幅が、前記導体パターンの幅より大きく、かつ導体パターンの外縁より外側に突出して形成されていることを特徴とする。

【0008】

(2) 本発明の積層型チップインダクタは、前記(1)において、

前記コイル状導体を積層方向に透視した形状が長方形または長円形をなし、該コイル状導体の長辺部に前記スルーホールとの接合部が形成されていることを特徴とする。

【0009】

(3) また、本発明の積層型チップインダクタは、前記(1)において、

前記コイル状導体を積層方向に透視した形状が長方形または長円形をなし、該コイル状導体の短辺部または弧状部に前記スルーホールとの接合部の一部または全部が形成され、

積層方向に透視して見た場合、前記端子電極は前記導体パターンを覆わず、前記スルーホールとの接合部の外側への突出部の少なくとも一部を覆う構造を有することを特徴とする。

【0010】

(4) また、本発明の積層型チップインダクタは、前記(1)ないし(3)のいずれかにおいて、

前記スルーホールとの接合部の面積がスルーホールの断面積の2倍以上の広さに形成されていることを特徴とする。

【発明の効果】

【0011】

本発明の積層型チップインダクタは、導体パターンのスルーホールとの接合部を、導体パターンの外縁より外側に突出させ、内側には突出させずに幅広に形成したので、コイル状導体で発生するフラックスをスルーホールとの接合部によって阻害する度合が大幅に減少する。このため、コイルの重要特性であるQを向上させることが可能となる。

【0012】

また、前記コイル状導体を積層方向に透視した形状を長方形または長円形とし、該コイル状導体の長辺部に前記スルーホールとの接合部を形成した場合には、導体パターンが積層体の側面(切断面)に露出したり、端子電極が導体パターンに短絡する度合いが大幅に

減少し、歩留まりが向上する。

【0013】

また、前記コイル状導体が長方形または長円形をなす場合、積層方向に透視して、前記端子電極は前記導体パターンを覆わず、前記スルーホールとの接合部の外側への突出部の少なくとも一部を覆う構造とすれば、端子電極とスルーホールとの接合部との間の容量結合の度合いが減少し、自己共振周波数（SRF）の低下を抑制することができる。

【0014】

また、スルーホールとの接合部の面積をスルーホールの断面積の2倍以上（好ましくは4倍以下）とすることにより、スルーホールの位置精度と、スクリーン印刷等の位置精度から発生するお互いのずれを吸収し、コイルとしての断線を防止することができる。

【発明を実施するための最良の形態】

【0015】

図1は本発明による積層型チップインダクタの一実施の形態を、積層方向に透視して見た図である。図1において、1は積層体、2はその中に形成されたコイル状導体であり、図2の積層構造図に示すように、前記コイル状導体2は1／2ターン構造の導体パターン2a～2fをスルーホール3a～3eによって接続することにより構成される。4a、4bは積層体1の積層方向に略直角をなす長手方向の両端部に設けられた端子電極であり、これらの端子電極4a、4bに積層方向の両端の導体パターン2a、2fの引き出し導体5a、5bにそれぞれ接続される。

【0016】

6a～6eは前記スルーホール3a～3e上に導体パターン2a～2eと同時に形成される接合部である。7a～7eは積層により前記スルーホール3a～3eが重ねられる接合部である。これらの接合部6a～6e、7a～7eは、導体パターン2a～2fの外縁より外側に一部が突出し内側には突出しないように、図3に導体パターン2bで代表して示すように、導体パターン2a～2eの幅W3より接合部6a～6e、7a～7eの幅W4を広く設定する。好ましくは、前記接合部6a～6e、7a～7eの面積（L・W4）をスルーホール3a～3eの断面積の2倍以上、好ましくは4倍以下として接合部6a～6e、7a～7eとの位置ずれを防止する。

【0017】

この積層型チップインダクタは、複数個取りのためのセラミックグリーンシート1a～1jを準備し、そのうち、導体パターン2a～2f間の絶縁層1c～1gを形成するグリーンシートにスルーホール3a～3eをあける。次に絶縁層1c～1hに相当するグリーンシートに銀や銅ペーストからなる導体ペーストにより導体パターン2a～2fを印刷する。その印刷の際に、スルーホール3a～3eに導体ペーストを充填し、積層する。その後、縦横に切断して例えば使用した金属粉材料に適した温度、環境で焼成し、両端に導体ペーストを焼き付けし、その後、はんだ付けのための電気めっきを施す。

【0018】

このように、スルーホール3a～3eとの接合部6a～6e、7a～7eを積層体1の外側に突出した幅広形状にすれば、コイル状導体2に発生するフラックスの通過が接合部6a～6e、7a～7eによって妨げられる度合いが大幅に減少するので、Q値が向上する。

【0019】

また、仮に、図1に示すように、長方形をなすコイル状導体2の長辺部に設けた接合部6a（～6e）、7a（～7e）と積層体1の側面との間に間隔Sが形成されるように設計した場合において、従来構造を踏襲して、図4に示すように、間隔Sと同様の間隔がコイル状導体2と積層体1の側面との間に形成されるように構成した場合、印刷による導体パターンのにじみやパターンのずれにより導体パターンが2点鎖線に示すように積層体1の側面に露出したり、端子電極4a、4bと短絡する可能性が大きくなる。

【0020】

一方、本実施の形態の構造を採用すると、長方形をなすコイル状導体の長辺の一部にの

み幅広の接合部6 a～6 e、7 a～7 eが形成されているので、導体が積層体1の側面に露出したり、端子電極4 a、4 bに短絡する可能性が非常に小さくなり、歩留まりが大幅に向上する。前記接合部6 a～6 e、7 a～7 eは、コイル状導体2の長辺部の端部に設けてもよいが、これらの接合部6 a～6 e、7 a～7 eをコイル状導体2の長辺部の中央付近に設けることが、前記にじみ等による端子電極4 a、4 bと導体パターン2 a～2 fとの短絡の可能性を少なくする意味において好ましい。

【0021】

また、図1から分かるように、積層方向に見て長方形をなすコイル状導体2の短辺側が端子電極4 a、4 bによって覆われないようにコイル状導体2を配置することにより、コイル状導体2と端子電極4 a、4 bとの容量結合の度合いが減少し、SRFの低下を防止することができる。

【0022】

図5は本発明の他の実施の形態であり、図6はその層構造図である。図5、図6において、1 a～1 iは積層体1を構成する絶縁層、2 g～2 kはコイル状導体2を1/2ターンごとに構成する導体パターン、3 f～3 iはスルーホール、4 c、4 dは導体パターン2 g、2 kの引き出し導体5 c、5 dを接続する端子電極、6 f～6 iはスルーホール3 f～3 iの部分に充填される導体ペーストと共に印刷により形成されるスルーホールとの接合部、7 f～7 iは積層によりスルーホール3 f～3 iが接合される接合部である。

【0023】

これらの接合部6 f～6 i、7 f～7 iは前記実施の形態と異なり、積層方向に見て長方形をなすコイル状導体2の短辺部にコイル状導体2の外縁より外側に一部が突出するように形成されている。また、図5に示すように、積層方向に透視して、前記端子電極4 c、4 dは前記導体パターン2 g～2 kの短辺部を覆わず、前記スルーホール3 f～3 iとの接合部6 f～6 i、7 f～7 iの外側への突出部の少なくとも一部を覆う構造を有する。この実施の形態の積層型チップインダクタも、前記同様の製造方法により作製される。

【0024】

このように構成すれば、前記実施の形態と同様に、接合部6 f～6 i、7 f～7 iがコイル状導体2の内側に突出しないので、フラックスと接合部6 f～6 i、7 f～7 iによる通過障害の度合いが減少し、Qの向上が達成できる。また、端子電極4 c、4 dとスルーホールとの接合部6 f～6 i、7 f～7 iとの間の容量結合の度合いが減少し、SRFの低下を防止することができる。

【0025】

図7は本発明の他の実施の形態であり、図8はその層構造図である。図7、図8において、1 a～1 jは積層体1を構成する絶縁層、2 m～2 rはコイル状導体2を3/4ターンごとに構成する導体パターン、3 j～3 nはスルーホール、4 e、4 fは導体パターン2 m、2 rの引き出し導体5 e、5 fを接続する端子電極、6 j～6 nはスルーホール3 j～3 nの部分に充填される導体ペーストと共に形成されるスルーホールとの接合部、7 j～7 nは積層によりスルーホール3 j～3 nが接合される接合部であり、これらの接合部6 j～6 n、7 j～7 nは前記実施の形態と異なり、積層方向に見て長方形をなすコイル状導体2の短辺部と長辺部の双方にコイル状導体2の外縁より外側に一部が突出するように形成されている。

【0026】

また、図7に示すように、積層方向に透視して、前記端子電極4 e、4 fは前記導体パターン2 m～2 rを覆わず、前記スルーホール3 j～3 nとの接合部6 j～6 n、7 j～7 nの外側への突出部の少なくとも一部を覆う構造を有する。この実施の形態の積層型チップインダクタも、前記同様の製造方法により作製される。

【0027】

この実施の形態においても、前記実施の形態と同様に、Qの向上と、SRFの低下の抑制効果があげられる。また、図7、図8の実施の形態によれば、図1、図2の実施の形態に比較してコイル状導体2の長辺部からの接合部6 j、7 j、6 l、7 l、6 n、7 nの

突出数がターン数（図2の場合は3.5ターン、図8の場合は4.5）の割に少なくなり（図2の場合は長辺部における接合部の突出数が10個、図8の場合は6個）、歩留まりの向上が期待できる。

【0028】

また、図5、図6の実施の形態に比較しても、コイル状導体2の短辺部における接合部6k、7k、6m、7mの突出数も、ターン数（図6の場合2.5ターン、図8の場合4.5ターン）の割には少なくなり、SRF低下の抑制効果が図5、図6の場合に比較して高くなる。

【0029】

前記各実施の形態においては、積層方向に透視した場合のコイル状導体2の形状を長方形としたが、長円形としてもよい。

【0030】

本発明の構造は、従来の積層型チップインダクタに比較し、コイル状導体2が積層体1の外周側より内側に位置することから、従来のものよりコイル状導体2全体の線路長がやや短くなるので、インダクタンス値についていえば、比較的小さいインダクタンス値を得るもの（インダクタンス値が10nH以下）に適用する場合に好適なものである。

【実施例】

【0031】

（実施例1）多数個取り用のセラミックグリーンシートとして、ストロンチウム、カルシウム、アルミナ、酸化珪素からなるガラス70wt%、アルミナ30wt%の組成のセラミック組成物を含むものを用いた。この多数個取り用のグリーンシートに、図1、図2の実施の形態の形状を実現するためのスルーホール3a～3eを設けた後、銀ペーストの印刷により、導体パターン2a～2fをそれぞれ対応する多数個取り用のグリーンシートに印刷すると共に、前記スルーホール3a～3eに銀ペーストを充填した。これらのグリーンシートを積層した後、完成寸法が1005（長辺が1.0mm、幅および高さが0.5mm）となるようにチップ単体に切断し、900℃で焼成した。その後、端子電極4a、4bの下地層となる銀ペーストを700℃で焼付けし、さらにNiとSnとを電気めっきにより被着した。焼成後の導体パターン2a～2fの幅は50μm、接合部6a～6e、7a～7eの幅を80μm、導体パターン2a～2fの厚みを12μm、コイル状導体2の内径を長手方向が320μm、短手方向が150μm、導体パターン2a～2fを介在させない絶縁層1a～1jの厚みを30μm、絶縁層1c～1jにおける導体パターン2a～2fを介在させた部分の厚みを20μm、ターン数を3.5とし、インダクタンス値が3.3nHとなるように構成した。

【0032】

また、比較例として、接合部6a～6e、7a～7eの幅を前記と同様とし、その突出方向を内側にしたものとし、他の構成は前記実施例と同じにしてインダクタを構成した。

【0033】

図9は前記実施例Aと比較例Bについて、10MHzから3000MHzの範囲において、Q値を測定した結果を示すグラフである。図9から明らかなように、本発明の実施例による場合、比較例に比較して、携帯電話で使用される周波数範囲（800～3000MHz）において、Q値が6から10優れている。

【0034】

（実施例2）

図5、図6に示した実施の形態の構造をとるインダクタにおいて、コイル状導体2の幅、ターン数を前記実施例1と同じにし、インダクタンス値が3.3nHとなるものにおいて、コイル状導体2の位置を変え、

（1）積層方向に透視した場合、接合部6f～6i、7f～7iが端子電極4c、4dに覆われない場合

（2）積層方向に透視した場合、接合部6f～6i、7f～7iの一部が端子電極4c、4dに覆われた場合

(3) 積層方向に透視した場合、接合部 6 f ~ 6 i 、 7 f ~ 7 i の全部が端子電極 4 c 、 4 d に覆われた場合

についてそれぞれSRFを調べたところ、(1) の場合 : 6 . 8 GHz 、 (2) の場合 : 6 . 3 GHz 、 (3) の場合 : 5 . 9 GHz の結果が得られ、接合部が端子電極 4 c 、 4 d によって覆われる度合いを少なくすることが、SRFの低下を防止する意味で重要であることが判明した。

【図面の簡単な説明】

【0035】

【図1】本発明による積層型チップインダクタの一実施の形態を積層方向に透視して見た図である。

【図2】図1の積層型チップインダクタの層構造図である。

【図3】図1の積層型チップインダクタのスルーホールとの接合部の構造を示す平面図である。

【図4】比較例の導体パターンの説明図である。

【図5】本発明による積層型チップインダクタの他の実施の形態を積層方向に透視して見た図である。

【図6】図5の積層型チップインダクタの層構造図である。

【図7】本発明による積層型チップインダクタの他の実施の形態を積層方向に透視して見た図である。

【図8】図7の積層型チップインダクタの層構造図である。

【図9】本発明の実施例と比較例の周波数に対するQ値を比較して示すグラフである。

【図10】従来の積層型チップインダクタの一例を積層方向に透視して見た図である。

【図11】従来の積層型チップインダクタの他の例を積層方向に透視して見た図である。

【図12】(A) 、 (B) 、 (C) は従来の積層型チップインダクタのスルーホールとの接合部を示す図である。

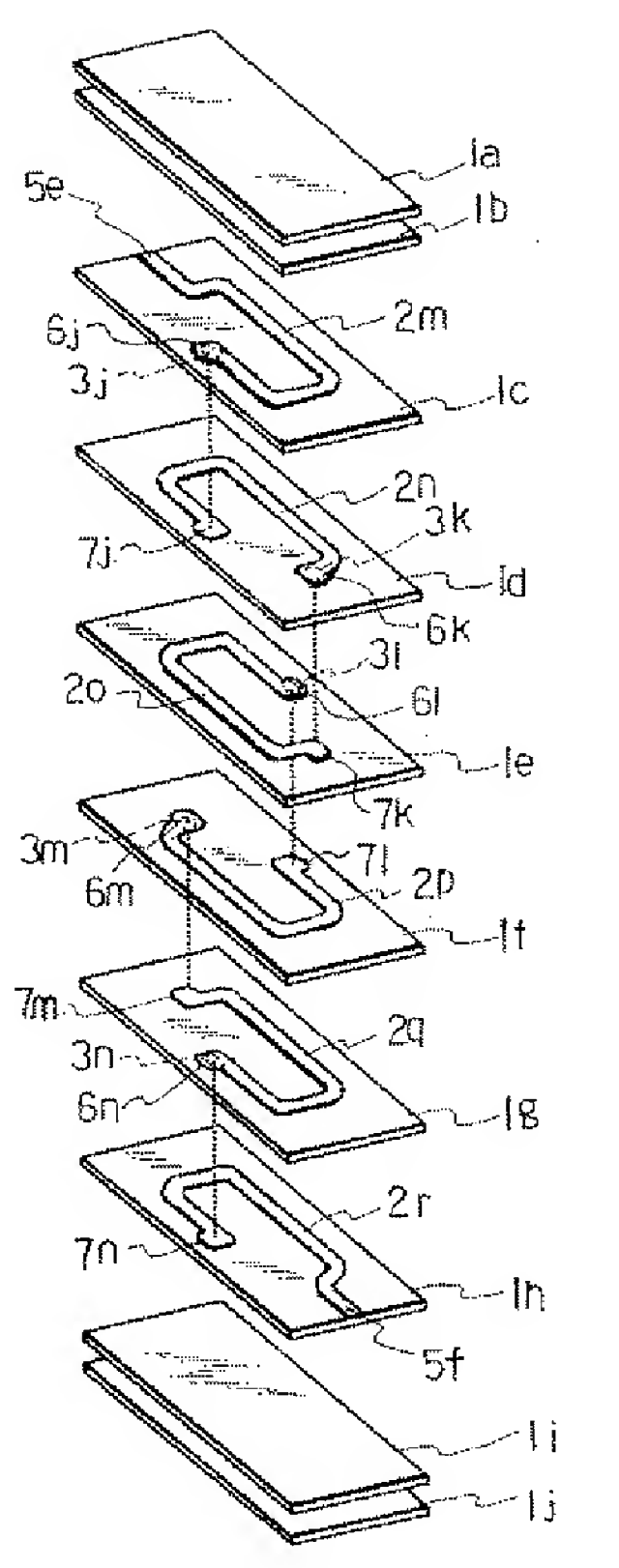
【図13】従来の積層型チップインダクタにおけるフラックスの流れを示す図である。

【符号の説明】

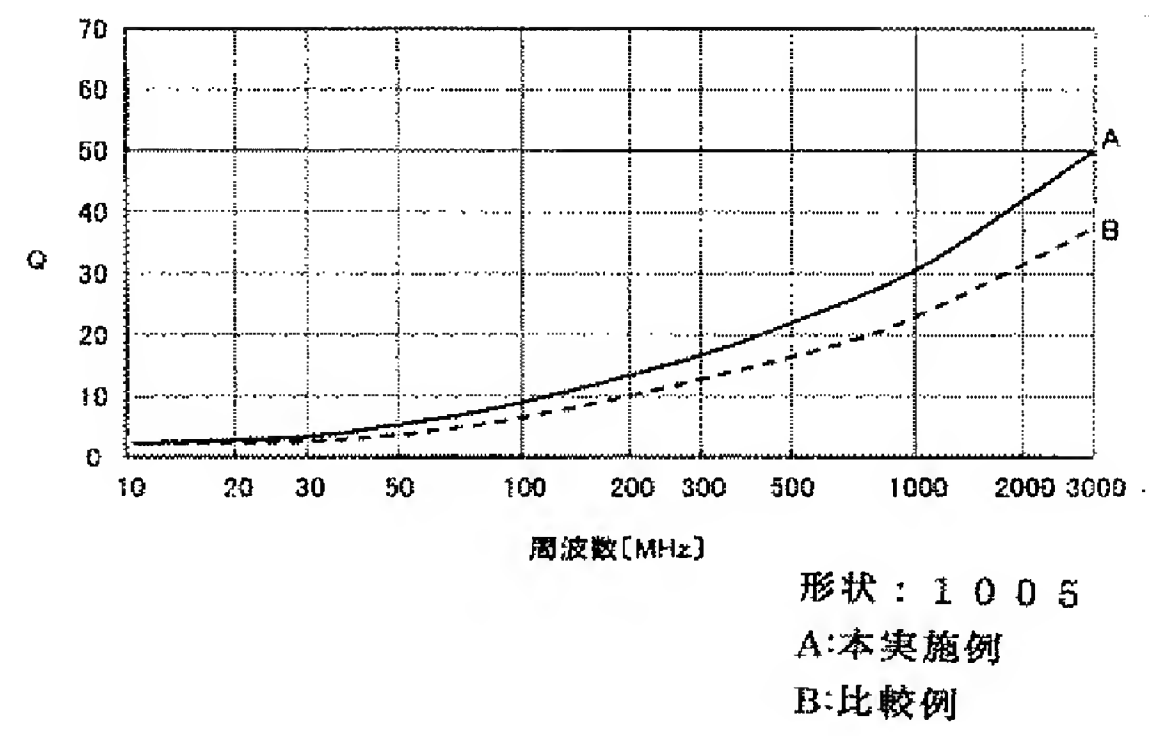
【0036】

1 : 積層体、1 a ~ 1 j : 絶縁層、2 : コイル状導体、2 a ~ 2 r : 導体パターン、3 a ~ 3 n : スルーホール、4 a ~ 4 f : 端子電極、5 a ~ 5 f : 引き出し導体、6 a ~ 6 n 、 7 a ~ 7 n : 接合部

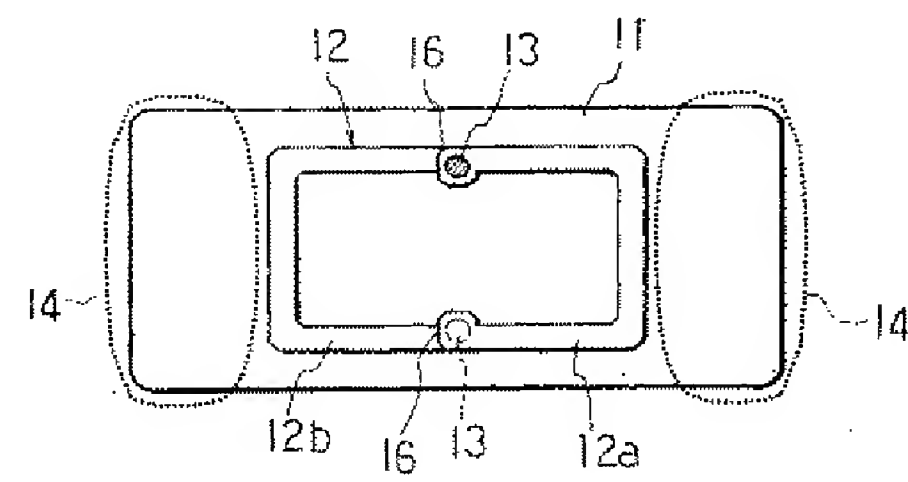
【図8】



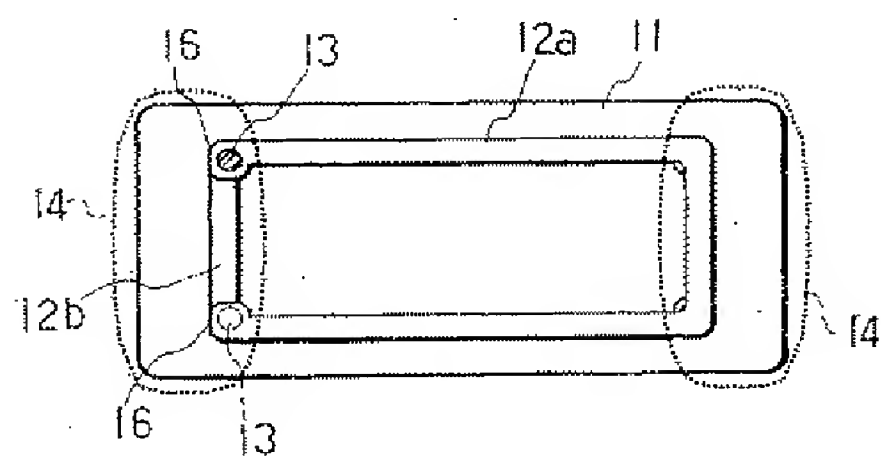
【図9】



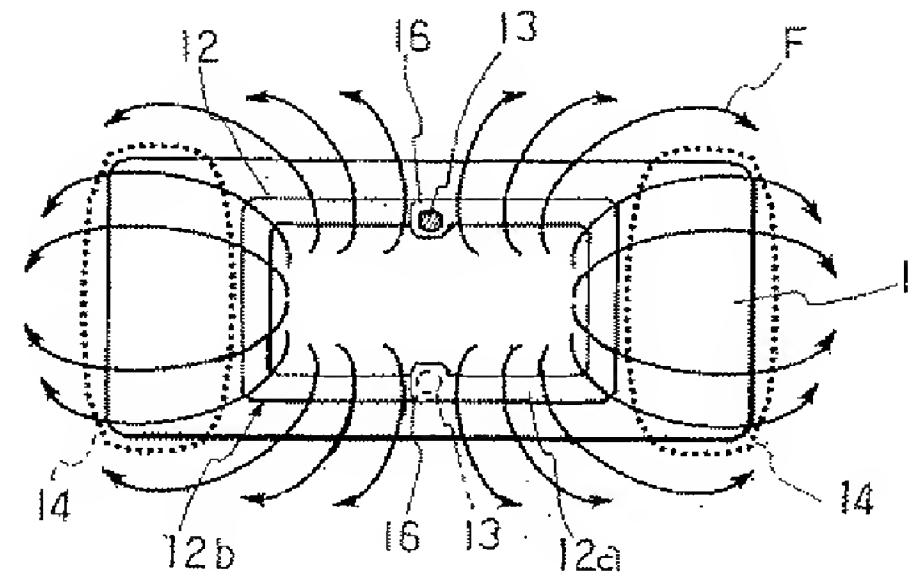
【図10】



【図11】



【図13】



【図12】

